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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/164,123	09/30/1998	ALBRECHT MAYER	GR-97-P-2681	6288

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EXAMINER
MALDONADO, JULIO J

ART UNIT	PAPER NUMBER
2823	

DATE MAILED: 05/20/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/164,123	MAYER, ALBRECHT	
	Examiner	Art Unit	
	Julio J. Maldonado	2823	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 January 2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-11 and 16-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-11 and 16-18* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

1. The final rejection as set forth in paper No.20 is withdrawn in response to applicants' amendments.

2. A new rejection is made as set forth in this Office Action.

3. Claims 1-11 and 16-18 are pending in the application.

Continued Examination Under 37 CFR 1.114

4. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 03/11/2003 has been entered.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claim 1 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kuriyama (U.S. 5,682,057) in view of Hatanaka (U.S. 5,587,598).

In reference to claims 1, 2 and 18, Kuriyama (Figs.1-4) in a related method to form a fuse structure teaches providing a first integrated circuit chip (7, 8) having a terminal (12) and a signal terminal (11); forming an electrically conductive connection

(10) between the terminal (12) and the signal terminal (11) of the first integrated circuit chip (7, 8); providing a second integrated circuit chip (3) having a terminal (3c) that is coupled to the first integrated circuit chip (7, 8); disposing the first integrated circuit chip (7, 8) and the second integrated circuit chip (3) adjacent one another; electrically joining the signal terminal (11) of the first integrated circuit (7, 8) to the terminal (3c) of the second integrated circuit chip (3), wherein said joining comprises using an electrically conductive material; connecting the terminal (12) of the first integrated circuit chip (7, 8) to a terminal (5) of a package (17); and subsequent to connecting the terminal (12) of the first integrated circuit chip (7, 8) to the terminal (12) of the package (17), severing the electrically conductive connection (10) between the terminal (12) and the signal terminal (11) of the first integrated circuit chip (7, 8) using an energy pulse (column 2, line 64 – column 5, line 61). Kuriyama also teach providing a protective structure that becomes conductive to dissipate electrostatic discharge (column 5, lines 51 – 61).

Kuriyama fails to teach providing the second integrated circuit chip having a terminal that is coupled to the protective structure. However, Hatanaka (Figs.1-5) in a related method to form a fuse structure teach providing a protective structure (23, 24) that becomes conductive to dissipate electrostatic discharge; and providing an integrated circuit chip having a terminal (10) that is coupled to the protective structure (23, 24) (column 3, line 5 – column 4, line 67). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to form a protection structure as taught by Hatanaka in the fuse formation method of Kuriyama to arrive at

the claimed invention, and furthermore, to control potential variations of the semiconductor device (column 4, line 61 – column 5, line 4).

Still, Kuriyama fails to teach said severing step performed by applying an electrical pulse. However, Hatanaka teaches wherein the severing step if performed by applying an electrical current pulse to the terminal of the integrated circuit chip (Hatanaka, column 4, lines 18 – 21). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Kuriyama and Hatanaka to enable the severing step to be performed by applying an electrical current pulse.

In reference to claim 3, the combined teachings of Kuriyama and Hatanaka teach forming the electrically conductive connection with a portion of reduced cross sectional area as compared to the rest of the connection; and dimensioning the portion to dissipate electrostatic discharges between the terminal and the signal terminal of the first integrated circuit chip and to be severed during application of the energy pulse in the severing step (Kuriyama, Fig.1 and Hatanaka, Figs.1A-2A, column 3, line 5 – column 4, line 67).

In reference to claims 4-7, 16 and 17, the combined teachings of Kuriyama and Hatanaka teach wherein the energy pulse used in the severing step is an electrical current pulse or a laser beam applied to the terminal of the second integrated circuit chip; disposing the first integrated circuit chip and the second integrated circuit chip in a package having terminal pins so that the signal terminal of the first integrated circuit chip is not accessible from outside of the package, wherein said disposing sep is

performed so that terminal of the second integrated circuit chip is not covered by the first integrated circuit chip; connecting the terminal of the first integrated circuit chip and the terminal of the second integrated circuit chip to a respective terminal pin of the package; and wherein the severing step is performed after the step of connecting the respective terminals to the respective terminal pins (Kuriyama, Figs.1-2 and column 3, lines 4 – 49).

7. Claims 8-11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kuriyama (U.S. 5,682,057) in view of Hatanaka (U.S. 5,587,598) and the applicants admitted prior art.

Kuriyama (Figs.1-4) in a related method to form a fuse structure teaches providing a first integrated circuit chip (7, 8) having a terminal (12) and a signal terminal (11); forming an electrically conductive connection (10) between the terminal (12) and the signal terminal (11) of the first integrated circuit chip (7, 8); providing a second integrated circuit chip (3) having a terminal (3c) that is coupled to the first integrated circuit chip (7, 8); disposing the first integrated circuit chip (7, 8) and the second integrated circuit chip (3) adjacent one another; electrically joining the signal terminal (11) of the first integrated circuit (7, 8) to the terminal (3c) of the second integrated circuit chip (3), wherein said joining comprises using an electrically conductive material; connecting the terminal (12) of the first integrated circuit chip (7, 8) to a terminal (5) of a package (17); and subsequent to connecting the terminal (12) of the first integrated circuit chip (7, 8) to the terminal (12) of the package (17), severing the electrically conductive connection (10) between the terminal (12) and the signal terminal (11) of the

first integrated circuit chip (7, 8) using an energy pulse (column 2, line 64 – column 5, line 61). Kuriyama also teach providing a protective structure that becomes conductive to dissipate electrostatic discharge (column 5, lines 51 – 61).

Kuriyama fails to teach providing the second integrated circuit chip having a terminal that is coupled to the protective structure. However, Hatanaka (Figs.1-5) in a related method to form a fuse structure teach providing a protective structure (23, 24) that becomes conductive to dissipate electrostatic discharge; and providing an integrated circuit chip having a terminal (10) that is coupled to the protective structure (23, 24) (column 3, line 5 – column 4, line 67). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to form a protection structure as taught by Hatanaka in the fuse formation method of Kuriyama to arrive at the claimed invention, and furthermore, to control potential variations of the semiconductor device (column 4, line 61 – column 5, line 4).

Still, Kuriyama fails to teach said severing step performed by applying an electrical pulse. However, Hatanaka teaches wherein the severing step if performed by applying an electrical current pulse to the terminal of the integrated circuit chip (Hatanaka, column 4, lines 18 – 21). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Kuriyama and Hatanaka to enable the severing step to be performed by applying an electrical current pulse.

The combined teachings of Hatanaka and Kuriyama fail to explicitly teach providing a protective structure acting as a switch that becomes conductive when there

is an overvoltage to dissipate an electrostatic discharge to a line for a supply voltage. However, the prior art teaches a method to provide electrical connection including providing a protective structure acting as a switch that becomes conductive when there is an overvoltage to dissipate an electrostatic discharge to a line for a supply voltage instant. (page 2, lines 4 – 13). Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention was made to provide the protective structure as taught by the prior art in the ESD protection method of Hatanaka and Kuriyama, since this would prevent electrostatic discharges that come into contact with the outer circuitry (page 2, lines 4-8).

In reference to claims 9-11, the combined teachings of Kuriyama and Hatanaka teach that the electrically joining step is performed using an electrically conductive solderable or adhesive material; and including electrically joining the other one of the first and second terminal pads of the second integrated circuit chip (Hatanaka, column 3, line 5 – column 6, line 11).

Response to Arguments

8. Applicant's arguments with respect to claims 1-11 and 16-18 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

9. Papers related to this application may be submitted directly to Art Unit 2823 by facsimile transmission. Papers should be faxed to Art Unit 2823 via the Art Unit 2823 Fax Center located in Crystal Plaza 4, room 3C23. The faxing of such papers must conform to the notice published in the Official Gazette, 1096 OG 30 (15 November

1989). The Art Unit 2823 Fax Center number is **(703) 305-3432**. The Art Unit 2823 Fax Center is to be used only for papers related to Art Unit 2823 applications.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to **Julio J. Maldonado** at **(703) 306-0098** and between the hours of 8:00 AM to 4:00 PM (Eastern Standard Time) Monday through Friday or by e-mail via julio.maldonado@uspto.gov. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Olik Chaudhuri, can be reached on (703) 306-2794.

Any inquiry of a general nature or relating to the status of this application should be directed to the **Group 2800 Receptionist** at **(703) 308-0956**.

JMR
5/10/03

George Fourson
Primary Examiner